

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL L. HEFLIN

Appeal No. 95-3125
Application 08/071,920¹

HEARD: May 6, 1998

Before THOMAS, JERRY SMITH, and BARRETT, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134
from the examiner's rejection of claims 1-12, which constitute

¹ Application for patent filed June 3, 1993.

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all the claims in the application. Amendments after final rejection were filed on July 7, 1994 and August 2, 1994. Both of these amendments were entered by the examiner. These amendments resulted in the withdrawal of rejections made under 35 U.S.C.

§ 112 in the final rejection [advisory action, Paper #8].

The disclosed invention pertains to a control system having a plurality of distributed input/output interface modules. Specifically, information is provided to a plurality of input/output devices by way of a host interface connected to a plurality of secondary interfaces. The host interface and each secondary interface has a hardware controlled multinode interface (HCMI). An address counter in each secondary HCMI directly controls activation of that HCMI.

Representative claim 1 is reproduced as follows:

1. In a control system having a plurality of distributed input/output interface modules, comprising

a central processing unit (CPU) for controlling information to and from a plurality of input/output devices,

a host interface having a host hardware controlled multinode interface (HCMI);

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a plurality of secondary hardware interfaces each having a secondary HCMI;

data and control transmission line means parallel connected to each of said HCMI's;

said CPU having means for transmitting and receiving data and control bytes of information employed to control said plurality of input/output devices;

said bytes of information comprising a data byte, an error byte and an address/command byte which defines the absence or presence of another data byte as well as the address of the input/output device being addressed, and

a HCMI address counter in each said secondary HCMI which defines the unique address of the secondary HCMI with which the host HCMI is to communicate, whereby

said bytes of information communicated to or from said CPU and an input/output device are active when the address counter activates a unique secondary HCMI.

The examiner relies on the following reference:

Ketelhut et al. (Ketelhut)	4,764,868	Aug. 16, 1988
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Claims 1-12 stand rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers Ketelhut taken alone.

Rather than repeat the arguments of appellant or the examiner, we make reference to the briefs and the answer for the respective details thereof.

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OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellant's arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-12. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S.

1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

With respect to independent claims 1 and 11, the examiner basically finds that Ketelhut discloses all the features of these claims except for the address counter in

each of the secondary hardware interfaces. The examiner generally concludes that the claimed address counter would have been obvious in view of Ketelhut because such elements are well known and common in the art and such elements would make Ketelhut's system more efficient and flexible [answer, pages 5-6]. Appellant argues that Ketelhut does not teach the hardware controlled multinode interfaces as recited in claims 1 and 11. Appellant also argues that Ketelhut does not teach or suggest the bytes of information as recited in claim 1. Finally, appellant argues that the address counter as recited in independent claims 1 and 11 is neither taught nor suggested by Ketelhut.

At the outset we observe that Ketelhut is basically exemplary of the type of distributed input/output controller which appellant describes as the prior art. In particular, Ketelhut uses a programmed central processing unit (software) for the host interface [element 20] and for each of the secondary interfaces [element 36]. Although any central processing unit is a combination of hardware and software components, it is clear from appellant's description of the

invention that a programmed computer would not be considered to be a "hardware controlled multinode interface" as that term is used by appellant.

The interfaces recited in claims 1 and 11 would correspond to the connections between computer 20 and computers 36 in Ketelhut. Ketelhut does not describe how these two computers are interconnected except to note that the connection is by way of an interface port. No description of this interface port is offered in Ketelhut. Although Ketelhut does disclose hardware components as forming part of each of the I/O points within each module, this hardware would not meet the limitations of the interfaces recited in these claims.

Claim 1 recites that the bytes of information comprise "a data byte, an error byte and an address/command byte which defines the absence or presence of another data byte as well as the address of the input/output device being addressed." The examiner argues that communications in Ketelhut are inherently by way of bytes of information. Although it is probably correct that communications in Ketelhut use

successive bytes of information, claim 1 requires more than this. Claim 1 recites that the bytes of data must indicate a specific relationship of the bytes of data as well as the address of the input/output device being addressed. This relationship is best illustrated by Figures 6A and 6B of the application. Even if Ketelhut is presumed to transmit information in the form of bytes, there is no suggestion whatsoever that these bytes would be arranged to convey information in the form and manner specifically recited in claim 1.

Claims 1 and 11 recite that the address counter in each secondary HCMI defines the unique address which is used to activate the associated secondary HCMI. Although the various I/O modules in Ketelhut must be addressable, the addressing of these modules is clearly contained within the microprocessors 36 rather than in an address counter as claimed. There is also no address counter in the I/O points of Ketelhut because the microprocessor 36 is shown connected to each I/O point by separate, dedicated lines [see Figure 3]. Although the examiner has asserted that such address counters

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would have been obvious to the artisan, the present record does not support the use of address counters in the specific manner recited in the claims.

As we noted above, Ketelhut is really typical of what appellant has described as the background of the invention. Although Ketelhut will control a plurality of input/output devices just as appellant's invention controls a plurality of input/output devices, appellant's result is achieved by a combination of structure which is different from the structure disclosed by Ketelhut. We are not in a position to say whether there is factual evidence available which might suggest the obviousness of the structure as claimed by appellant. What we can say is that the only evidence of record in this case does not teach or suggest the structure as recited in appellant's claims.

In summary, the structure as specifically recited in independent claims 1 and 11 is not taught or suggested by the distributed input/output system of Ketelhut. Therefore, we do not sustain the rejection of claims 1 and 11 or of claims 2-10

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and 12 which depend therefrom. The decision of the examiner
rejecting claims 1-12 is reversed.

REVERSED

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Administrative Patent Judge)	
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Jerry Smith)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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)	
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